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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,120	02/03/2004	Clarence Chui	5093-006	4288

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EXAMINER	
LEWIS, DAVID LEE	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
02/25/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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	Application No.	Applicant(s)	
Office Action Summary	10/772,120	CHUI, CLARENCE	
	Examiner	Art Unit	
	David L. Lewis	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Miles (2006/0262126).**

As in claim 1, Mlles teaches of a display system, **figures 4 and 9**,

comprising: a standardized display driver to provide address voltages, **figure 9 item 926**;

an array of interferometric elements, **figure 9 item 930**;

and a voltage adjuster to adjust address voltages to provide adjusted row address voltages to the array of interferometric elements, **figure 9 items 924 and 928**.

As in claim 2, Mlles teaches of the standardized display driver further comprising a driver for a liquid crystal display, paragraph 45, emissive display.

As in claim 3, Mlles teaches of the array of interferometric elements further comprising an array of iMoD.TM. elements, paragraph 5.

As in claim 4, Mlles teaches of the voltage adjuster further comprising a resistor divider network to lower the address voltage amplitudes, figure 9 items 924 and 928.

As in claim 5, Mlles teaches of the voltage adjuster to adjust row address voltages, figure 9 item 924.

As in claim 6, Mlles teaches of the voltage adjuster to adjust column address voltages, figure 9 item 928.

As in claim 7, Mlles teaches of method of manufacturing an array of modulator elements and an adjuster circuit, **figures 4, 9, 18 and 19**,

comprising: depositing a first metal layer on a transparent substrate, **paragraph 133-138**;

patterning and etching the first metal layer to form electrodes, **paragraph 133-138**;

depositing an optical stack layer, **paragraph 133-138**;

depositing a first sacrificial layer upon the optical stack layer, **paragraph 133-138**;

depositing a second metal layer on the sacrificial layer, **paragraph 133-138**;

and patterning and forming the second metal layer to form modulator elements, **paragraph 133-138**;

forming resistors from one metal layer and connecting the resistors with a subsequent metal layer, **paragraph 133-138, paragraph 128 item 1805**.

As in claim 8, Mlles teaches of forming the resistors from one metal layer further comprising forming the resistors from the first metal layer and connecting the resistors with the second metal layer, **paragraph 133-138**.

As in claim 9, Mlles teaches of further comprising: depositing a second sacrificial layer; depositing a third metal layer on the second sacrificial layer; and

patterning and etching the third metal layer to form posts and supports, **paragraph 133-138**.

As in claim 10, Mlles teaches of forming the resistors further comprising forming the resistors from the first metal layer and connecting the resistors using the third metal layer, **paragraph 133-138**.

As in claim 11, Mlles teaches of forming the resistors further comprising forming the resistors from the second metal layer and connecting the resistors using the third metal layer, **paragraph 133-138**.

As in claim 12, Mlles teaches of further comprising: depositing a third sacrificial layer; depositing a fourth metal layer on the third sacrificial layer, **paragraph 133-138**; patterning and etching the fourth metal layer to form a bus layer, **paragraph 133-138**.

As in claim 13, Mlles teaches of forming the resistors from one metal layer further comprising forming the resistors from the first metal layer and connecting the resistors using the fourth metal layer, **paragraph 133-138**.

As in claim 14, Mlles teaches of forming the resistors from one metal layer further comprising forming the resistors from the second metal layer and connecting the resistors using the fourth metal layer, **paragraph 133-138**.

As in claim 15, Mlles teaches of forming the resistors from one metal layer further comprising forming the resistors from the third metal layer and connecting the resistors using the fourth metal layer, **paragraph 133-138**.

2. **Claims 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Stumbo et al. (2006/0256059).**

As in claim 16, Stumbo et al. teaches of resistor network, **figure 3B**,

comprising: an incoming address line, **figure 3B items line between transistors 310A and 330A**;

a first resistor connected between the address line and a conductive bus, **figure 3B item 310A** (drain/source transistor resistance and line resistance), conductive bus coming from the control circuitry;

and a second resistor connected between the address line and an adjusted address line, **figure 3B item 322** (drain/source transistor resistance and line resistance).

As in claim 17, Stumbo et al. teaches of the address line further comprising a row address line, figure 3B item 350A.

As in claim 18, Stumbo et al. teaches of the address line further comprising a column address line, figure 3B item 340A.

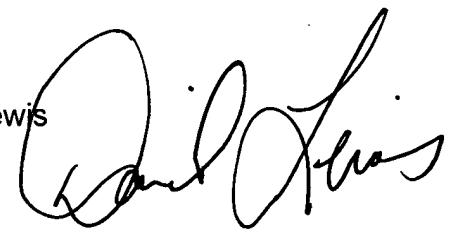
Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis

February 19, 2008



Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :5/05a; 5/05b; 5/05c; 5/05d; 6/05; 9/05; 11/06; 2/08; .